Arav Raghunathan

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Education

Georgia Institute of Technology — Atlanta, GA

Bachelor of Science in Electrical Engineering, Minor in Computing & Intelligence — *Expected in May 2028*

Experience

Software Engineering Intern — May 2026 - August 2026

SoloPulse Co. — *Peachtree Corners, GA*

- Independently architected and developed the entire proof-of-concept system for a U.S. Army ADAS contract as the sole engineer on the project, with progress reviewed and approved by engineering leadership through ongoing check-ins.
- Engineered a distributed **gRPC-based network** connecting a NUC to 6 NVIDIA Jetsons, building a C++ system manager and API controller with a custom TCP image streamer to support real-time status monitoring and image streaming.
- Configured dnsmasq and systemctl across 6+ Linux edge devices to streamline networking and deployment within a **10+ person company.**

Undergraduate Research Assistant — January 2026 – Present

ICE Lab @ Georgia Tech — *Atlanta, GA*

- Designing and developing **Field-Programmable Analog Arrays (FPAAs)** in SkyWater's 130 nm CMOS process for Vector Matrix Multiplication (VMM), supporting the lab's goal to develop efficient ML systems.
- Simulating analog circuits in Xschem and **Ngspice** and created corresponding layouts in Magic, translating designs from concept to physical implementation.
- Verifying design integrity using **LVS**, ensuring alignment between schematic and fabricated layout.

Peer Instructor — January 2026 – Present

The Hive Makerspace — *Atlanta, GA*

- Supported a high-traffic makerspace serving **1,000+** students, advising on hands-on technical skills including breadboarding and PCB fabrication.
- Mentored students on 3D printing (Bambu, Resin), circuit analysis, and laser cutting, fostering hands-on creativity and technical confidence.

ASIC Physical Design Engineer — January 2026 - Present

SiliconJackets — *Atlanta, GA*

- Independently designing and implementing a **32-bit RTL calculator**, including a custom datapath architecture and SRAM-based result storage, with the design cleared through internal review.
- Supporting **ASIC tapeout workflows** as part of the Physical Design team, collaborating on processes to meet project deadlines.
- Developing advanced proficiency in **SystemVerilog**, Cadence Virtuoso, and Innovus Stylus, applying these tools to complex digital design and physical implementation tasks.

Software Development Intern — August 2024 - May 2025

Oracle Corporation — *Suwanee, GA*

- Executed collaborative software projects utilizing **Oracle APEX**, developing resources for financial tracking and organization.
- Researched and synthesized industry papers on cloud computing's impact on healthcare, presenting to build shared understanding of emerging industry trends.

Projects

32-Bit RTL Calculator | *SystemVerilog, Cadence Design, Innovus Stylus, Python, Linux*

- Engineered the conceptual and physical design of a calculator that performs bit-wise addition.
- Leveraged SystemVerilog and Innovus Stylus to build a complete framework with testbench-based verification.

Technical Skills

Programming Languages: Java, Python, MATLAB, C, C++, RISC-V, SQL, PL-SQL, SystemVerilog, Linux
Hardware Design & Embedded Systems: Xschem, Ngspice, Magic, LVS (Layout Versus Schematic), Breadboading, Waveform Analysis, Arduino, ESP32, FGPA/FPAA Design, Signal Processing
Tools & Softwares: PTC Onshape, Oracle Application Express, Microsoft Office, Git, GDB, GCC, Dnsmasq, Systemctl